

What is claimed is:

- 1 1. A clock phase interpolator circuit comprising:
 - 2 a first plurality of differential transistor pairs, a first plurality of select
 - 3 transistors, and a first current source, the first current source coupled to each of the
 - 4 first plurality of differential transistor pairs through one of the first plurality of select
 - 5 transistors; and
 - 6 a second plurality of differential transistor pairs, a second plurality of select
 - 7 transistors, and a second current source, the second current source coupled to each of
 - 8 the second plurality of differential transistor pairs through one of the second plurality
 - 9 of select transistors.
- 1 2. The clock phase interpolator circuit of claim 1 wherein each differential
- 2 transistor pair is configured to receive a different phase of a clock signal.
- 1 3. The clock phase interpolator circuit of claim 2 further comprising a control
- 2 circuit to select one of the first plurality of differential transistor pairs and one of the
- 3 second plurality of differential transistor pairs.
- 1 4. The clock phase interpolator circuit of claim 3 wherein the first and second
- 2 current sources are variable current sources.
- 1 5. The clock phase interpolator circuit of claim 4 wherein the control circuit
- 2 includes output nodes coupled to the first and second current sources to control
- 3 currents sourced thereby.
- 1 6. The clock phase interpolator circuit of claim 4 wherein the first current source
- 2 comprises a plurality of parallel-coupled current source transistors, each being
- 3 individually selectable.

1 7. The clock phase interpolator circuit of claim 2 further comprising a
2 differential amplifier coupled to output nodes of both the first and second plurality of
3 differential transistor pairs.

1 8. The clock phase interpolator circuit of claim 7 wherein the first and second
2 current sources are constant current sources.

1 9. A clock recovery circuit comprising:
2 an input clock node and an output clock node;
3 a first circuit to generate multiple clock phases from a clock signal on the
4 input clock node;
5 a phase detector and control circuit to compare a phase of a data signal and a
6 phase of a clock signal on the output clock node, and to create interpolator control
7 signals; and
8 an interpolator circuit with a plurality of differential transistor pairs operative
9 to switch current responsive to the multiple clock phases and interpolator control
10 signals, to drive an output clock on the output clock node.

1 10. The clock recovery circuit of claim 9 wherein the interpolator circuit
2 comprises:
3 a first differential transistor pair responsive to a first clock phase, and
4 a second differential transistor pair responsive to a second clock phase.

1 11. The clock recovery circuit of claim 10 wherein the interpolator circuit further
2 comprises:
3 a first current source coupled to the first differential transistor pair; and
4 a second current source coupled to the second differential transistor pair.

1 12. The clock recovery circuit of claim 11 wherein the first and second current
2 sources are variable current sources responsive to the interpolator control signals.

1 13. The clock recovery circuit of claim 9 wherein the first and second current
2 sources are constant current sources.

1 14. The clock recovery circuit of claim 9 wherein the interpolator circuit further
2 comprises:

3 a first plurality of differential transistor pairs having differential output nodes
4 coupled in common;

5 a first current source coupled to source current through the first plurality of
6 differential transistor pairs;

7 a second plurality of differential transistor pairs having differential output
8 nodes coupled in common with the differential output nodes of the first plurality of
9 differential transistor pairs;

10 a second current source coupled to source current through the second
11 plurality of differential transistor pairs; and

12 a differential amplifier coupled to the differential output nodes to drive the
13 output clock on the output clock node.

1 15. The clock recovery circuit of claim 14 further comprising a separate select
2 transistor coupled between each differential transistor pair and a respective current
3 source, the select transistors being responsive to the interpolator control signals.

1 16. The clock recovery circuit of claim 9 wherein the first and second current
2 sources are fixed current sources.

1 17. The clock recovery circuit of claim 9 wherein the first and second current
2 sources are variable current sources having input nodes responsive to the interpolator
3 control signals.

1 18. An integrated circuit comprising:
2 a first differential transistor pair to receive a first clock signal at a first phase,
3 the first differential transistor pair having a first differential output node;
4 a second differential transistor pair to receive a second clock signal at a
5 second phase, the second differential transistor pair having a second differential
6 output node coupled in common with the first differential output node;
7 a first variable current source coupled to the first differential transistor pair;
8 a second variable current source coupled to the second differential transistor
9 pair; and
10 a differential amplifier having a differential input node coupled to the first
11 differential output node.

1 19. The integrated circuit of claim 18 further comprising:
2 a third differential transistor pair coupled in parallel with the first differential
3 transistor pair between the first differential output node and the first current source.

1 20. The integrated circuit of claim 19 further comprising:
2 a fourth differential transistor pair coupled in parallel with the second
3 differential transistor pair between the second differential output node and the second
4 current source.

1 21. The integrated circuit of claim 20 further comprising:
2 a first select transistor coupled between the first differential transistor pair
3 and the first current source;
4 a second select transistor coupled between the second differential transistor
5 pair and the second current source;
6 a third select transistor coupled between the third differential transistor pair
7 and the first current source; and
8 a fourth select transistor coupled between the fourth differential transistor
9 pair and the second current source.

1 22. The integrated circuit of claim 21 further comprising a control circuit to
2 select one of the first and second select transistors, and one of the third and fourth
3 select transistors, and to select a first current to be provided by the first current
4 source, and to select a second current to be provided by the second current source.

1 23. The integrated circuit of claim 18 further comprising a delay locked loop
2 circuit coupled to the first and second differential transistor pairs, to provide the first
3 and second clock signals from a received clock signal.

1 24. The integrated circuit of claim 23 further comprising a phase detector having
2 input nodes coupled to an output node of the differential amplifier and to a data node
3 to receive a data signal, and having an output node to provide a phase error signal.

1 25. The integrated circuit of claim 24 further comprising a control circuit to
2 receive the phase error signal and to control the first and second variable current
3 sources.

1 26. The integrated circuit of claim 25 wherein the phase comparator provides a
2 digital error signal.

1 27. The integrated circuit of claim 25 wherein the phase comparator provides an
2 analog error signal.

1 28. The integrated circuit of claim 27 wherein the control circuit includes an
2 analog-to-digital converter.